PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Data Storage Apparatus

We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to data storage apparatus. In manufacturing memories for data storage, it is found that some of the memories produced are not perfect, that is to say, some of their bit positions are not capable of reliably storing data. A common practice is to test the memories after manufacture and reject or repair the imperfect ones. However, several data storage systems have been proposed in which a supplementary store (which may be an alternative storage area in the main memory) is used to store a word which is assigned to a word location in the main memory which contains faulty bit positions. In some of those systems the word is stored both correctly in the supplementary store and also incorrectly in the faulty word location in the main memory. Upon read-out either just the word in the supplementary store is read out or corresponding words are read out from both the supplementary store and the main memory and a discriminator is used to give precedence to the word stored in the supplementary store.

According to the invention, data storage apparatus includes a main memory comprising a plurality of word locations each containing a plurality of bit positions, a supplementary store arranged to store data bits which are assigned to faulty bit positions in the main memory, and selection means responsive when a main memory word location containing one or more faulty bit positions is addressed, to address one or more word locations in the supplementary store, to establish a one-for-one relationship between the faulty bit positions in the main memory word location and bit positions in the addressed supplementary store word location or locations and to access only those bit positions in the addressed supplementary store word location or locations which, by virtue of the aforesaid one-for-one relationship, correspond to the one or more faulty bit positions in the main memory word location.

How our invention can be carried into effect will now be described by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a block diagram of a first data storage apparatus embodying the invention;

Figure 2 is a block diagram of a second data storage apparatus embodying the invention;

Figure 3 is a block diagram of a third data storage apparatus embodying the invention;

Figure 4 is a block diagram of a fourth data storage apparatus embodying the invention;

Figure 5 is a diagram of a matrix switch used in the apparatus of Figure 4; and

Figure 6 is a block diagram of a fifth data storage apparatus embodying the invention.

A data storage apparatus (Figure 1) includes a main memory 1 comprising a plurality of word locations each containing a plurality of bit positions. The main memory has 4096 word locations, each of 144 bit positions. Operably associated with the main store 1 is a memory address register 2 in which a representation of the address of a

word location in the main memory 1 can be set up, a main memory address decoder 3 and a data register 4 capable of storing 144 bits. The data register 4 is functionally divided into four sections 4a, 4b, 4c, and 4d, each of thirty-six bit positions, and the main store word locations are functionally divided into four sections 1a, 1b, 1c, and 1d, corresponding respectively to sections 4a, 4b, 4c and 4d of the data register. The apparatus also includes a supplementary store 5 having word locations in each of four similar segments 5a, 5b, 5c and 5d, operably associated with sections 4a, 4b, 4c and 4d of the data register respectively. Thus each supplementary store word location contains 36 bit positions. Two-way gates 6 control the transfer of data between the supplementary store 5 and the data register 4. Operably associated with the supplementary store 5 is a supplementary address decoder 7 arranged to be responsive to a binary representation of a supplementary store address location read from a word stored in an associative memory 8. Each word stored in the associative memory 8 comprises a tag portion having twelve bit positons, a flag bit portion (the purpose of which will be described below) having thirty-six bit positions and an address portion having sufficient bit positions to store the address of any word location in the supplementary store. Each word in the associative memory 8 is associated with a respectitve word location containing faulty bits in the main memory 1. A word driver 9 is arranged to read a word from a word location in the associative memory 8 when the address of a corresponding word location in the main memory is set up in the memory address register 2. The supplementary address decoder 7 serves to drive the supplementary store word location having the address defined by the address portion of a word read from the associative memory 8.

Some of the word locations in the main memory 1 may contain faulty bit positions in which bits of data cannot be reliably stored and sensed. The apparatus of Figure 1 can be arranged so as to be reliably operable despite such faults in the main memory 1, provided that all the faulty bit positions in any word location are contained within only any one of the sections 1a, 1b, 1c and 1d of that word location. Bit positions in the supplementary store 5 are used to store the data bits which are assigned to faulty bit positions in the main memory 1.

The associative memory 8, the supplementary address decoder 7 and the two-way gates 6 constitute a selection means responsive when a main memory word location containing one or more faulty bit positions is addressed, to address a word location in the supplementary store and to establish a one-for-one relationship between the faulty bit positions in the main memory word location and bit positions in the addressed supplementary store word location. The flag bit portion of each word in the associative memory 8 is used to identify which bit position or positions in the supplementary store word location identified in the address portion of that associative memory word contain the data bit or bits to complete a word stored in the main memory word location identified in the tag portion of that associative memory word.

The apparatus is set up for the operation in the following manner. A diagnostic program is used to determine which word locations in the main memory 1 contain faulty bit positions in just one section of the sections 1a to 1d and to identify those faulty bit positions. (Any word location which has faulty bit positions in more than one section should not be used at all). For each main memory word location having faulty bit positions in just one section, a word is recorded in the first free word location in the associative memory 8. It is arranged that the tag portion of that word contains the address of the main memory word location, the flag bit portion defines the faulty bit positions in that main memory word location, the most significant bits of the address portion define the supplementary store segment associated with the same section of the data register 4 as the main memory word section containing the faulty bit positions and the remaining bits of the address portion contain the address of the first word location in the defined supplementary store segment which contains free bit positions corresponding to those defined by the flag portion. For example, the diagnostic program may determine that word location 20 contains faulty bit positions in section 1b and that those faulty bit positions are numbers 39 and 64 counting from the first bit position in the word, that is, numbers 3 and 28 counting from the first bit position in section 1b. It will be assumed that it is known that the first word location in the second segment 5b of the supplementary store, in which both bit positions number 3 and number 28 are free, is word location number 18. Accordingly the following word is recorded in the first available word location (say number 13) in the associative memory: — 20 in the tag portion; bits 3 and 28 marked in the flag portion; and two recorded in the two most significant bit positions and 18 in the remaining bit positions in the supplementary address portion.

When words have been recorded in the associative memory corresponding to all the main memory word locations which have faulty bit positions in only one section, the apparatus is ready to store data. Data is written into the apparatus as follows. The

binary representation of a main memory word location address is set up in the memory address register 2, for example, under the control of the central processing unit of a computer, and a data word is set up in the data register 4. The data word is then read into the addressed main memory word location under the control of the main decoder 3. If the word location contains a section having faulty bit positions, the tag portion of a word in the associative memory 8 will match the contents of the memory address register 2. Upon recognition of such a match, the word driver 9 reads out the flag portion and address portion. The address from the address portion is decoded by the auxiliary decoder 7 and the supplementary store word location having that address is energized. The set bits read from the flag portion control the enabling of the two-way gates 6, more particularly, each set bit enables four of the two-way gates 6, which are operably associated with corresponding bit positions in each of the register sections 4a to 4d.

As each supplementary store segment is operably associated with only one section of the data register, only bits set in that data register section associated with the segment containing the addressed supplementary store word location can be read into that location. Further, the only bits which can be so read in are those that can pass the gates 6. Thus the gates 6 enabled by the flap portion permit selected bits to be read from the data register section associated with the supplementary store word location addressed by the address portion into bit positions in that supplementary store word location. For example, if the memory address register 2 is set to contain the address of main memory word location 20 and a word is set in the data register, the main decoder 3 will cause that word to be read into word location 20. At the same time, a match will be recognized between the contents of the memory address register 2 and the tag portion of the word in associative memory word location 13, resulting in read-out of its flag and address portions by the word driver 9. The address portion contains the address of word location number 18 in supplementary store segment 5b. Read-out of the flag portion enables the two-way gates 6 associated with data register bit positions numbers 3 and 28 (section 4a); 39 and 64 (section 4b) 75 and 100 (section 4c); and 111 and 136 (section 4d). As no word location in the supplementary store segments corresponding to data register sections 4a, 4c and 4d is addressed, only data bits from the data register bit positions 39 and 64 pass through the enabled gates 6 to bit positions 3 and 28 in supplementary store word location 18. Thus bit positions 3 and 28 in supplementary store word location 18 store data bits to complete the word stored in main memory word location 20.

The bit positions other than numbers 3 and 28 in word location 18 of segment 5b can be used to store bits to complete words stored in main memory word locations other than number 20. For example, bit positions 1, 8, 9, 10 and 24 may store bits to complete a word in main memory word location 23 and bit locations 2, 4, 23 and 30 may store bits to complete a word in main memory word location 24. It should be noted that the word locations in segment 5b can store bits only to complete sections of words in main memory section 1b as both segment 5b and section 1b have access only to data register section 4b.

Data is read from the storage apparatus in the following manner. A binary representation of a main memory word location address is set up in the memory address register 2 and read-out of the word stored in that word location is initiated under the control of the main decoder 3. Simultaneously, if the addressed main memory word location has any faulty bit positions, the tag portion of an associative memory word will match the contents of the memory register 2 and that associative memory word will be read out. The two-way gates 6 will be enabled in accordance with the flag portion of that word and a supplementary store word location will be addressed under the control of the supplementary address decoder 7 in accordance with the address portion of that word. Thus, selected bits from the addressed supplementary store word pass through the enabled gates 6 to the data register 4. The non-enabled gates 6 prevent the passage of the remaining bits from that word into the data register.

The apparatus should be such that data bits from the supplementary store word location are set into the data register 4 before the data bits from the main memory word location enter the register. Thus, bits from faulty bit locations in the main memory word location cannot be set into the data register 4 as the data register bit positions to which they are directed will have been already set by bits from the supplementry store 5. This characteristic may arise because the access time of the supplementary store 5 is less than that of the main memory 1. That is to say, the word from the main memory word location having the address set up in the memory address register 2 reaches the data register 4 subsequently to the setting of the data register 4 by bits from the supplementary store 5.

As an alternative to arranging that data bits from the supplementary store word location are set into the data register 4 before bits from the main memory, a further set of two-way gates (not shown) can be connected between the main memory and the data regis-

ter 4 and provision made for those gates selectively to be inhibited in accordance with the flap portion which determines the enabling of the two-way gates 6.

The data storage apparatus of Figure 2 is generally similar to that of Figure 1, like parts in the two apparatuses being identified by the same reference designations. The main difference is that the word locations in the supplementary store 15 of Figure 2 are associated with the data register 4 in a different way to those of the supplementary store 5 of Figure 1. Each word location (of 36 bit positions) in the supplementary store 15 is operably associated with an adjacent pair of half sections of the data register 4 (each section of which contains 36 bit positions). In other words, half of the bit positions in each supplementary store word location is operably associated with one half section of the data register and the other half of the bit positions with an adjacent half section of the data register. Word locations operably associated with like pairs of adjacent register half sections are grouped in respective segments 15a to 15h of the supplementary store 15. As each word location is associated with two register half sections there are 8 supplementary store segments. Each segment contains 4 words. The first bit position of each word location in segment 15a co-operates with the first bit position in section 4a of the data register; the thirty-sixth bit position in that word location with the thirty-six bit position in register section 4a and the first bit position in each word location in segment 15b co-operates with the nineteenth bit position in register section 4a. Thus, segment 15a is operably associated with the pair of register half sections forming section 4a and segment 15b is associated with the second half of section 4a and the first half of section 4b. Apart from the connections to and from the supplementary store 15 arising from the segmenting arrangement just described, the apparatus of Figure 2 is like that of Figure 1.

The apparatus of Figure 2 can accommodate deficiencies arising from faulty bit positions in the main memory provided that all the faulty bit positions in any word location lie within just one of a plurality of predetermined groups of successive bit positions. Each group of 36 successive bit positions in the main memory word locations, which is operably associated with a pair of adjacent register half sections will be referred to herein as a "span". Provided that all the faulty bit positions in any main memory word location lie within a span, the deficiencies of the main memory 1 can be overcome. Thus, as any group of 19 successive bit positions must fall within a span, a single group of up to 19 faulty bit positions in a main memory word location can always be accommodated.

One word in the supplementary store may be used to "repair" up to 36 bits in the main memory as the combination of the address of a word in the supplementary store (which address defines a particular segment) and a flag bit (stored in the associative memory 8) uniquely allocates a bit position in the supplementary store 15 to replace a faulty bit position in the main memory 1. The apparatus is set up for operation in the following manner. A diagnostic program is used to determine which word locations in the main memory 1 contain faulty bit positions falling within a span, and to identify those faulty bit positions, (If all the faulty bit positions in any word location do not fall within a span, that word location should not be used at all, and it will be assumed that no word location is so defective). For each main memory word location having faulty bit positions falling within a span, a word is recorded in the first free word location in the associative memory 8. The tag portion of that word contains the address of the main memory word location, the flap portion defines (with reference to positions in register sections 4a to 4d) the faulty bit positions in a span of the main memory word location. The most significant bits of the address portion define the supplementary store segment containing word locations operably associated with the same pair of adjacent register half sections as the span, and the remaining bits of the address portion contain the address of the first word location in the defined supplementary store segment which contains free bit positions in the positions defined by the flag portion. For example, the diagnostic program may determine that bit position numbers 19 and 39 in main memory word location 20 are faulty. These two faulty bit positions are contained in a span operably associated with the second half of data register section 4a and the first half of section 4b. The word locations in supplementary store segment 15b are operably associated with that pair of adjacent register half sections and so the most significant bits of the supplementary address portion defines segment 15b and the remaining bits of that portion contain the address of the first word location in segment 15b which contains free bit positions at positions 1 and 21. It will be assumed that it is known that the first word location in segment 15b in which both bit positions numbers 1 and 21 are free in location number 3. Accordingly the following word is recorded in the first available word location (say number 14) in the associative memory:— 20 in the tag portion; bits 19 and 3 marked in the flag portion; and 2 recorded in the most significant bit positions and 3 in the remaining bit positions in the supplementary address portion. When words have been recorded in the associative memory corresponding to all the

main memory word locations which have faulty bit positions falling within a span, the apparatus is ready to store data. Data is written into the apparatus as follows, words are set up in the memory address register 2 and the data register 4. The data word is then read from the data register into the addressed main memory word location. If the word location contains a span having faulty bit positions, the tag portion of a word in the associative memory 8 will match the contents of the memory address register 2 and upon recognition of such a match the flag and address portions of that word will be read out. The supplementary store word location having the address defined by the address portion will be energized. That word location is operably associated with just one pair of adjacent data register half sections and accordingly bits can only be entered into that word location from that pair of data register half-sections. The set bits read from the flag portion control the enabling of the two-way gates 6; more particularly each set bit enables four of the two-way gates 6, which are operably associated with corresponding bit positions in each of the register sections 4a, 4b, 4c and 4d. The gates 6 enabled by the flag bit portion permit selected bits to be read from the adjacent pair of data register half-sections associated with the supplementary word location addressed by the address portion into bit positions in that supplementary store word location. For example, if the memory address register 2 is set to contain the address of main memory word location 20 and a word is set in the data register, the main decoder 3 will cause that word to be read into word location 20. At the same time a match will be recognized between the contents of the memory address register 2 and the tag portion of the word in the associative memory word location 14, resulting in the flag and address portions of that word being read out. The address portion contains the address of the word location number 3 segment 15b of the supplementary store. The flag portion results in the enabling of the two-two gates 6 associated with data register bit position numbers 3 and 19 (section 4a); 39 and 55 (section 4b) 75 and 91 (section 4c) and 111 and 127 (section 4d). As no word location in the addressed supplementary store segment spans bit positions 3, 55, 75, 91, 111 and 127 only data bits from the data register bit positions 19 and 39 pass through the enabled gates 6 to bit positions 1 and 21 in word location number 3 in segment 15b. Thus, bit positions 1 and 21 in that supplementary store word location store data bits to complete the word stored in main memory word location 20.

The bit positions other than numbers 1 and 21 in word location number 3 in segment 15b can be used to store bits to complete words stored in main memory word locations other than word location 20. It should be noted any given supplementary store word location can store bits to complete only sections of words comprising spans corresponding to the pair of adjacent register half-sections with which the segment containing that word location is associated.

Data is read from the apparatus in the following manner. A binary representation of a main memory word location address is set up in the memory address register 2 and read-out of the word stored in that word location is initiated under the control of the main decoder 3. Simultaneously, if the addressed main memory word location has any faulty bit positions a match will be recognized between the tag portion of a word in the associative memory 8 and the contents of memory address register 2 resulting in the two-way gates 6 being enabled in accordance with the flag portion of that word and a supplementary store word location will be addressed under the control of the supplementary address decoder 7 in accordance with the address portion of that word. Thus, selected bits from the addressed supplementary store word pass through the enabled gates 6 to the data register 4. The non-enabled gates 6 prevent the passage of the remaining bits from that word into the data register.

The number of bit positions in each supplementary store word location need not be one quarter of the number of bit positions in the main memory word locations. Conveniently, it may be 1/8, 1/6, 1/32 etc. of the main memory word length. The shorter the supplementary store word length the greater will be the number of segments into which the supplementary store word locations are divided and the shorter will be the spans in one of which all faulty bit positions in a main memory word location must fall for the apparatus to be capable of "repairing" the main memory. For example, if each main memory word location contains 144 bit positions and each supplementary store word location contains 18 bit positions, each section of the data register will be divided into 4 sub-sections, each of 9 bit positions. The flag portion of each associative memory work will therefore only need to contain 18 bits, but the supplementary store will have to be divided into sixteen segments.

Figure 3 is a diagram of a data storage apparatus including a main memory 31 comprising 4,096 word locations each containing thirty-six bit positions. Operably associated with the main memory 31 is a memory address register 32, a main memory address decoder 33 and a data register 34 capable of storing thirty-six bits. The data register 34 is functionally divided into four sections, 34a, 34b, 34c and 34d, each of nine bit positions. Each of two sections 35 and 36

of a supplementary store is divided into four similar segments, 35a, 35b, 35c, 35d and 36a, 36b, 36c, 36d respectively. Segments 35a and 36a are operably associated with data register section 34a segmetns 35b and 36b with section 34b, etc. Thus each word location in the supplementary store segments contains nine bit positions. Two-way gates 37a to 37d, and 38a to 38d control the transfer of data between the data register 34 and the supplementary store 35, 36. A first supplementary address decoder 39 for co-operation with supplementary store section 35 is arranged to be responsive to a representation of the address of a supplementary store location read from a portion of a word stored in an associative memory 41.

A second supplementary address decoder 40 is similarly associated with section 36 of the supplementary store and is arranged to respond to another portion of the same word read from the associative memory 41. Each word stored in the associative memory 41 comprises a tag portion having twelve bit positions, a first flag portion having nine bit positions, a first address portion having sufficient bit positions to store the address of any word location in supplementary store section 35, a second flag portion having nine bit positions, and a second address portion having sufficient bit positions to store the address of any word location in supplementary store section 36.

Each word in the associative memory 41 is associated with a respective word location in the main memory 31. A word driver 42 is arranged to read a word from a word location in the associative memory 41 when the address of a corresponding word location in the main memory is set up in the memory address register 32.

Provided that all the faulty bit positions in any main memory word location lie within any two spans of nine bit positions, which spans are operably associated with respective data register sections, the apparatus of Figure 3 can accommodate the deficiencies of the main memory. Two words in different sections of the supplementary store can be used to "repair" up to eighteen bits in the main memory as the combination of the address of a word in a supplementary store section, and a flag bit uniquely allocates a bit position in the supplementary store to replace a bit position in the main memory. The apparatus of Figure 3 is set up for operation in the following manner. A diagnostic program is used to determine which word locations in the main memory 31 contain faulty bit positions in only one or two nine-bit spans corresponding to data register sections, and to identify those faulty bit positions. (Any word location which has faulty bit positions which occupy more than two such nine-bit spans should not be used at all and it will be assumed that no word location is so defective). For each main memory word location having faulty bit positions in one nine-bit span or two nine-bit spans, a word is recorded in the first free word location in the associative memory 41. The tag portion of that word contains the address of the main memory word location. The first flag portion defines the faulty bit positions in one span of that main store word location. The most significant bits of the first address portion defines the supplementary store segment containing words operably associated with the one span containing the faulty bit positions and the remaining bits of that portion contains the address of the first word location in the defined supplementary store segment which contain free bit positions as defined by the first flag portion of that word. The second flap portion defines the faulty bit positions in the other span of the main memory word location, and the second address portion contains the address of a word location in the other supplementary store section. For example, the diagnostic program may determine that bit positions numbers 5 and 8, and 28 and 36 in main memory word location 20 are faulty. The first two of these faulty bit positions are contained in a span corresponding to data register section 34a and the second two of these fauty bit positions are contained in a span corresponding to data register section 34d. The word locations in supplementary store segments 35a and and 36a are operably associated with register section 34a and segments 35d and 36d with the register section 34d. It will be assumed that the first word location in segment 36a in which both bit positions numbers 4 and 8 are free is location number 3 and that the first word location in segment 35d in which both bit position numbers 1 and 9 are free is location number 2. Accordingly the following word is recorded in the first available word location (say number 4) in the associative memory 41:— 20 in the tag portion; bits 1 and 9 marked in the first flag portion; 4 (defining segment 35d) recorded in the two most significant bit positions and 2 (word location two) in the remaining bit positions in the first address portion; bits 5 and 8 marked in the second flag portion; and 1 recorded in the two most significant bit positions and 3 in the second address portion (segment 36a is the first segment in the second section of the supplementary store). When words have been recorded in the associative memory 41 corresponding to all the main memory word locations which have faulty bit positions within two spans of nine bit positions the apparatus is ready to store data.

A data word set up in the data register 34 is read into the main memory word location

defined by the address set up in the memory address register 32. If that word location contains one or two spans of faulty bit positions the tag portion of a word in the associative memory 41 will match the contents of the memory address register 32 and that word will be read out. Read-out of the first and second address portions of that word will result in energisation of the supplementary store word locations having these addresses. Each of those word locations is operably associated with just one register section and accordingly bits can only be entered into that word location from that register section. The set bits read from the first and second flag portions control the enabling of the two-way gates 37 and 38 respectively; more particularly each set bit enables four of the two-way gates, for example, one in section 37a, one in section 37b, one in section 37c, and one in section 37d. The enabled gates permit selected bits to be read from the data register sections associated with the supplementary word locations addressed by the first and second address portions into bit positions in those supplementary store word locations. For example, if the register 32 is set to contain the address of main memory word location 20 and a word is set in the data register 34, the main decoder 33 will cause that word to be read into word location 20. At the same time, a match will be recognized between the contents of the register 32 and the tag portion of the word in the associative memory word location 14, resulting in read-out of that word. Read-out of the first flag portion results in the enabling of the two-way gates 37 associated with data register bit position numbers 1 and 9 in each of the register sections and the read-out of the first address portion in the addressing of word location 2 in supplementary store segment 35d. Consequently, data bits from positions 1 and 9 in register section 34d pass through the enabled gates 37 to positions 1 and 9 in word location 2 in segment 35d. Thus, bit positions 1 and 9 in that supplementary store word location store data bits to "repair" the bits stored in bit positions 28 and 36 in main store word location 20. In a similar manner, read-out of the second flag and address portions result in bit positions 5 and 8 in word location 3 in segment 36a storing data bits to "repair" bits 5 and 8 of the word stored in main memory word location 20.

The bit positions other than numbers 1 and 9 in supplementary store word location 2 (segment 35d) can be used to store bits to complete words stored in main memory word locations other than word location 20. However, the supplementary store word locations 2 can only store bits to complete spans of main memory bit positions associated with section 34 of the data register.

Data is read from the apparatus in the following manner. A representation of a main memory word location address is set up in the register 32 and read-out of the word stored in that word location is initiated under the control of the main decoder 33. Simultaneously, if the addressed main memory word location has any faulty bit positions a match will be recognised between the tag portion of a word in the associative memory and the contents of the register 32, resulting in the two-way gates 37 and 38 being enabled in accordance with the first and second flag portions of that word and supplementary store word locations will be addressed under the control of the decoders 39 and 40 in accordance with the first and second addressed portions, respectively, of that word. Thus, selected bits from each of the addressed supplementary store word locations pass through the enabled gate 37 or 38 to the respective data register sections with which the word locations are operably associated. The gates 37 and 38 which are not enabled prevent the passage of the remaining bits from those word locations into the data register.

The number of bit positions in each supplementary store word location need not be one-quarter of the number of bit positions in the main store word location. Conveniently, it may be one-eighth, one-sixteenth, one-thirtysecond etc. of the number of bit positions in each main store word. The shorter the supplementary store word length the greater will be the number of segments into which the supplementary store word locations are divided and the shorter will be the data register sections in two of which all faulty bit positions in a main memory word location must fall for the apparatus to be capable of "repairing" the main memory. For example, if each main memory word location contains 144 bit positions and each supplementary store word location contains nine bit positions the data register would be divided into sixteen sections each of nine bit positions, and the supplementary store would be divided into thirty-two segments.

Two is not the maximum number of supplementary store segments that may be operably associated with one data register section. However, for each additional segment so associated the associative memory words would have to contain two additional portions, one a flag portion for marking selected bits in the word location in the additional supplementary store segment and one an address portion for storing the address of that word location.

A data storage apparatus (Figure 4) includes a main memory 51, a memory address register 52, a main address decoder 53, a data register 54, a supplementary store 55, and an associative memory 56. The apparatus of Figure 4 differs from that of Figures 1 to 3 in that instead of controlling two-way gates

between the data register and the supplementary store by means of a word read from the associative memory, the transfer of bits between the data register and the supplementary store is controlled by a matrix switch 57. The associative memory 56 is adapted to store words comprising only a tag portion and an address portion. A supplementary decoder 58 is used to address a word location in the supplementary store 55 in response to read-out of an address portion from a word in the associative memory 56. The switch matrix 57 is controlled by signals on control lines 60 energised upon read-out of words from the associative memory 56, there being a respective control line for each associative memory word location. The matrix switch 57 is settable to route any number of bits up to the capacity of a supplementary store word location to and from any of the bit positions in the data register 54. Thus, in operation, a particular word in the supplementary store 55 may contain say two bits associated with a first word in the main memory, three bits associated with a second word and a further three bits associated with yet another main memory word.

The apparatus is set up for operation in the following manner. First the word locations in the main memory 51 which contain faulty bit positions are determined. Let us assume that bit positions numbers 3 and 4 in main memory word location 327 are faulty and that the first word location in the supplementary store 55 which contains two previously unallocated bit positions (not necessarily adjacent) is location 7 and that those unallocated bit positions are numbers 6 and 7. The matrix 57 is set up to connect data register bit positions 3 and 4 with supplementary store bit positions 6 and 7 when a particular one of the control lines 60 is energised. Also, a word is stored in the associative memory 56 such that its tag portion contains the address of main memory word location 327 and its address portion contains the address of supplementary store word location 7. Read-out of that word from the associative memory is accompanied by energisation of that particular one of the control lines 60. Data is written into the apparatus as follows. The binary representation of a main store word location address is set up in the register 52 and a data word is set up in the data register 54. The data word is then read into the addressed main store word location under the control of the main decoder 53. If that word location contains faulty bit positions, the tag portion of a word in the associative memory 56 will match the contents of the memory address register 52 and so the word driver 59 reads out the address portion of that word and energizes a unique one of the control lines 60. That energized control line 60 sets up paths in the matrix switch 57 between data register bit positions and bit positions in the supplementary store word location defined by the address portion. For example, if the memory address register 52 is set to contain the address of main memory word location 327 and a word is set in the data register 54 the main decoder 53 causes that word to be read into word location 327. At the same time, a match will be recognised between the contents of the memory address register 52 and the tag portion of a word in the associative memory 56 resulting in read-out of the address portion which contains the address of word location 7 in the supplementary store 55. The data bits in register bit positions 3 and 4 are directed by the matrix 57 into bit positions 6 and 7 in supplementary store word location 7. It should be noted that all the data bits set into data register 54 are read into main memory word location 327 whereas only the data bits in bit position 3 and 4 are read into the supplementary store. Data is read from the storage apparatus in the following manner. A representation of a main memory word location address is set up in the register 52 and read-out of the word stored in that word location initiated under control of the decoder 53. Simultaneously, if the addressed main memory word location has any faulty bit positions, matching of an associative memory word tag portion and the contents of register 52 will be recognised and that associative memory word will be read out accompanied by energization of one of the control lines 60. Thus a word will be read out from the supplementary store 55 and selected bits from that word will be directed by the matrix 57 into bit positions of the data register 54 determined by which control line 60 was energised. Each data register bit position comprises a discriminator and latch designed to trigger on the first signal on its input exceeding a given threshold and to latch in that state. Thus, provided that a signal from the supplementary store arrives at the discriminator before a signal from a faulty bit position in the main memory the register position will be set in accordance with the signal from supplementary store and not in accordance with the signal from the main memory. Alternatively, the signal from the supplementary store can be arranged to override the signal from the main memory.

It is not necessary that the supplementary store should be perfect, i.e. having no faulty bit positions. The supplementary store can be tested to determine any faulty bit positions and use of such positions avoided. Thus, if the first bit in supplementary store word location 7 is faulty, it would not be used to store any bits to repair a word in the main memory 51.

A preferred form of the matrix switch 57 is represented in Figure 5. A set of 8 hori-

zontal lines 65, 65A are adapted to pass bit signals in parallel to and from a word location in the supplementary store 55. The lines 65 are intersected by a set of vertical lines 66, 66A which are adapted to convey bit signals to and from respective bit positions in the data register 54. Some of the control lines 60 are shown in Figure 5 and are referenced 60a to 60e. An intersecting pair of lines 65 and 66 may be connected through a transistor. For example line 65a is connected to line 66a via a transistor 68a, the emitter of transistor 68a being connected via diodes 69 to control lines 60a and 60e respectively. Similarly other pairs of intersecting lines 65 and 66 are connected at their intersections by transistors arranged to be energized by signals from selected ones of the control lines 60. In operation, when a signal is induced in either of control lines 60a or 60e transistor 68a is rendered conductive and if a signal arrives on line 65a the potential of line 66a changes.

Each of the embodiments so far described has included an associative memory to store the address of a word location in a supplementary store, used to store bits to repair bit positions in a main memory word location. The apparatus of Figure 6 does not include an associative memory but instead a main memory which is such that each word location can have recorded therein a word containing, in addition to the data portion, an address portion defining the address of a supplementary store word location and a flag portion identifying a particular bit position in that supplementary store word location. Thus, the apparatus of Figure 6 includes a main memory 81, a memory address register 82, a main decoder 83, a data register 84, a supplementary store 85 and a supplementary address decoder 86. Switch means 87 is arranged to control the transfer of bits between the data register 84 and the supplementary store 85. For each main memory word location containing faulty bit positions a representation of a supplementary store word location address is recorded in the address portion of that word and information defining the faulty bit positions in the main memory word location is recorded in the flag portion of that word. Having recorded information in the address and flag portions of all the word locations having faulty bit positions, the apparatus is ready for use. It should be noted that the information contained in the address and flag portions is retained throughout operation of the apparatus. Whenever a word is read from the main memory under the control of the main decoder 83 the address and flag portions are read out at well as the data portion. The contents of the data portion are passed to the data register 84. Read-out of the address portion results in the selection, via the decoder 86, and energization of a supplementary store word location and read-out of the flag portion sets the switch means 86 for transfer of bits between the supplementary store and the register 84. The supplementary store 85 may be divided into segments in a similar manner to the stores described in the apparatus of Figures 1, 2, or 3. If the supplementary store 85 were divided into segments in a similar manner to the store described in Figure 3 then each word location in the main memory would contain, in addition to the data portion, a pair of address portions defining the respective addresses of a pair of supplementary store word locations, and a corresponding pair of flag portions identifying particular bit positions in the respective supplementary store word locations. Further, the switch means 87 may be replaced by a switch matrix like that of the apparatus of Figure 4 and it would then not be necessary for the words in the main memory to include a flag portion as the switch matrix could be controlled by the signals on the word drive lines of the main memory 81.

WHAT WE CLAIM IS:—

1. Data storage apparatus including a main memory comprising a plurality of word locations each containing a plurality of bit positions, a supplementary store arranged to store data bits which are assigned to faulty bit positions in the main memory and selection means responsive when a main memory word location containing one or more faulty bit positions is addressed, to address one or more word locations in the supplementary store, to establish a one-for-one relationship between the faulty bit positions in the main memory word location and bit positions in the addressed supplementary store word location or locations, and to access only those bit positions in the addressed supplementary store word location or locations which, by virtue of the aforesaid one-for-one relationship, correspond to the one or more faulty bit positions in the main memory word location.

2. Apparatus as claimed in claim 1, in which the selection means is responsive to a signal representing the address of a main memory word location to address said one or more word locations in the supplementary store.

3. Apparatus as claimed in claim 2, in which the selection means includes an associative memory arranged to store words respectively corresponding to main memory word locations containing faulty bit positions, each associative memory word including a tag portion to store the address of the corresponding main memory word location and at least one address portion to store the address of a word location in the supplementary store.

4. Apparatus as claimed in claim 3, in which each associative memory word further

includes at least one flag portion to store data specifying the relationship between the bit positions in a supplementary store word location and some or all of the faulty bit positions in the main memory word location.

5. Apparatus as claimed in claim 4, in cludes a single address portion and a single which each associative memory word inflag portion to store the data specifying the relationship between the bit positions in the supplementary store word location and all the faulty bit positions in the main memory word location.

6. Apparatus as claimed in claim 1, in which each of the main memory word locations containing faulty bit positions includes at least one address portion arranged to store the address of a supplementary store word location and in which apparatus the selection means is responsive to read out of said address portion to address the supplementary store word location.

7. Apparatus as claimed in claim 6, in which each of the main memory word locations containing faulty bit positions further includes at least one flag portion arranged to store data defining the relationship between the bit positions in a supplementary store word location and some or all of the faulty bit positions in that main memory word location, and in which apparatus the selection means is responsive to read out of said flag portion to specify a one-for-one relationship between the faulty bit positions in that main memory word location and bit positions in the addressed supplementary store word location or locations.

8. Apparatus as claimed in claim 7, in which each of the main memory word locations containing faulty bit positions includes a single said address portion and a single said flag portion to store data defining the relationship between the bit positions in the supplementary store word location and all the faulty bit positions in the main memory word location.

9. Apparatus as claimed in any of the preceding claims, including a data register operably associated with the main memory so that data words can be transferred between the data register and locations in the main memory, and in which apparatus the supplementary store is divided into segments, the word locations being distributed amongst the segments, and in which each segment is operably associated with a section of the data register so that data bits can be transferred only between the associated sections and segments.

10. Apparatus as claimed in claim 9, in which the segments are associated with overlapping data register sections.

11. Apparatus as claimed in claim 9, in which a pair of segments is associated with each data register section.

12. Apparatus as claimed in any of claims 9 to 1, including a plurality of two-way switches for controlling the transfer of data between the supplementary store and the data register and means to set the switches in accordance with said one-for-one relationship specified by the selection means.

13. Apparatus as claimed in any of claims 9 to 11, including a matrix switch for controlling the transfer of data between the supplementary store and the data register and means to control the operation of the matrix switch in accordance with said one-for-one relationship specified by the selection means.

14. Data storage apparatus substantially as described herein with reference to Figure 1 of the accompanying diagrammatic drawings.

15. Data storage apparatus substantially as described herein with reference to Figure 2 of the accompanying diagrammatic drawings.

16. Data storage apparatus substantially as described herein with reference to Figure 3 of the accompanying diagrammatic drawings.

17. Data storage apparatus substantially as described herein with reference to Figure 4 of the accompanying diagrammatic drawings.

18. Data storage apparatus substantially as described herein with reference to Figure 6 of the accompanying diagrammatic drawings.

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1158010 COMPLETE SPECIFICATION
4 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

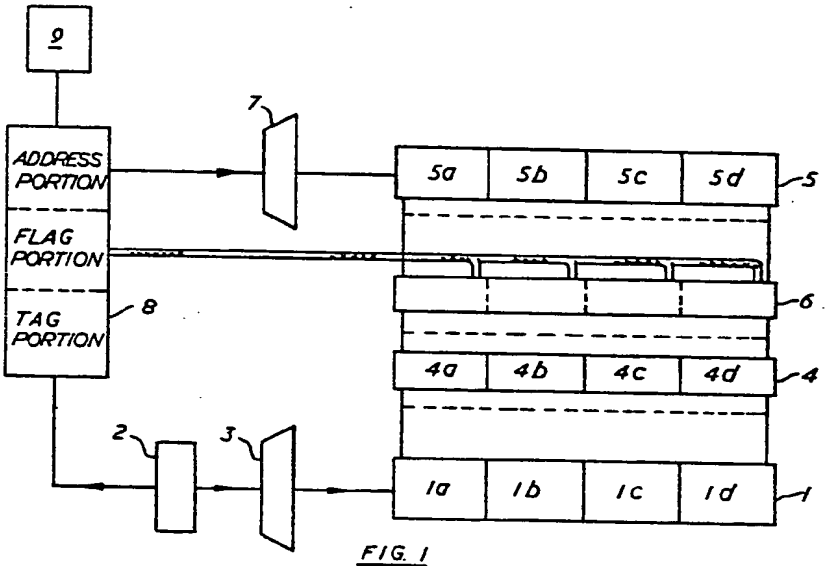

FIG. 1

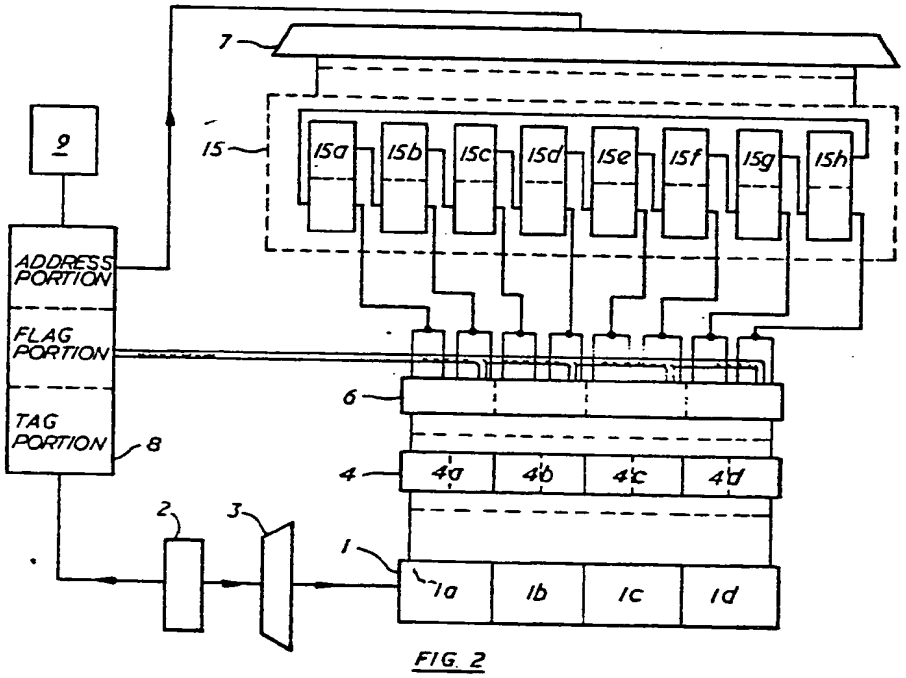

FIG. 2

1158010 COMPLETE SPECIFICATION

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Sheet 2

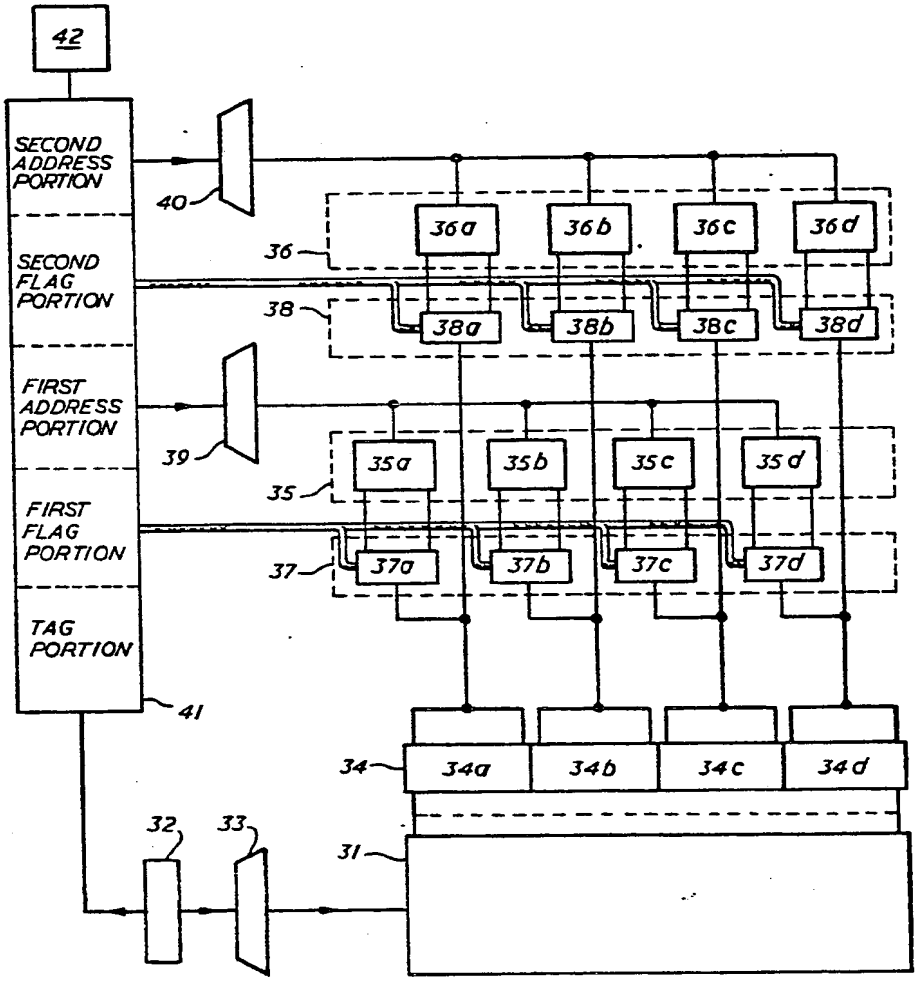

FIG. 3

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Sheet 3

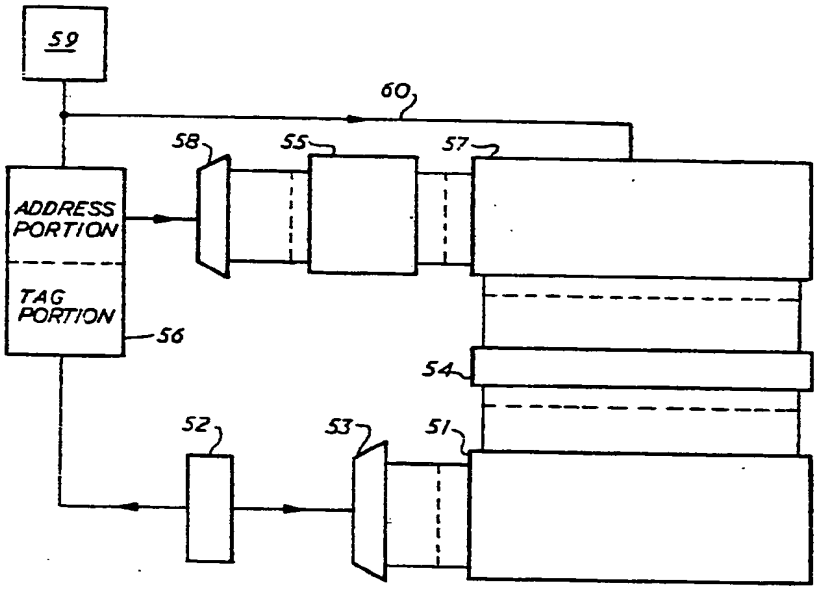

FIG. 4

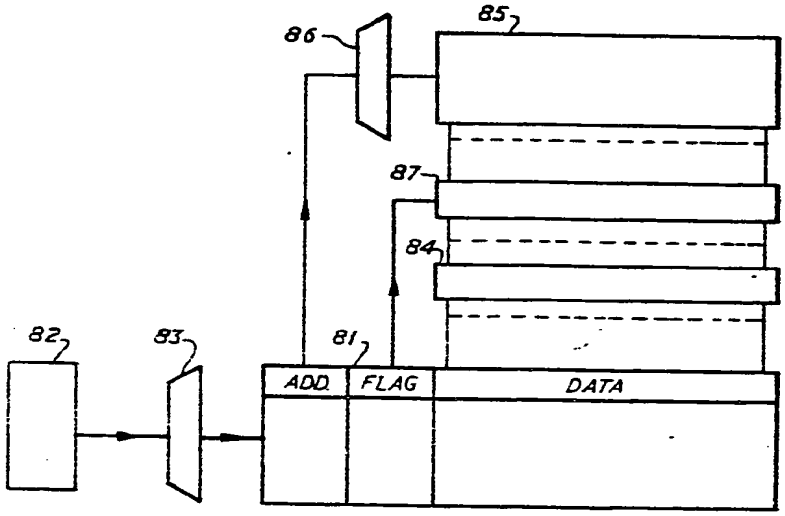

FIG. 6

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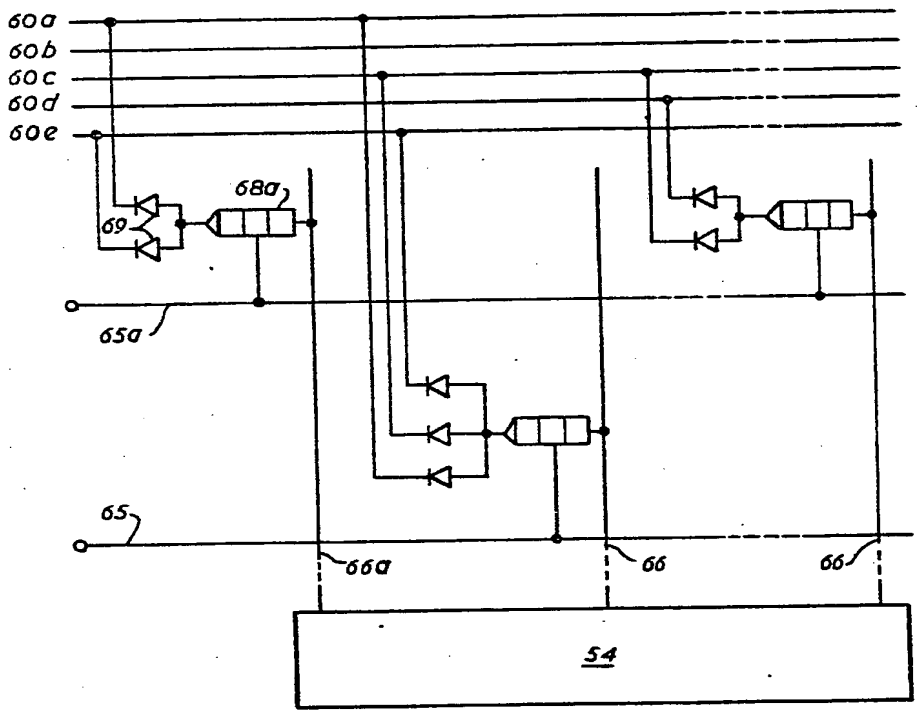

FIG 5